I^2C bus

Inter Integrated Circuits bus
by Philips Semiconductors

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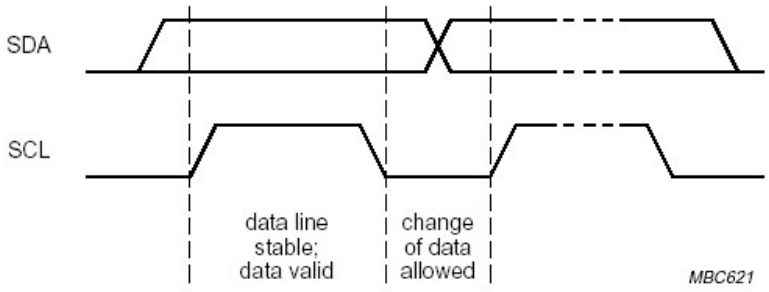
Basic Characteristics

- two-wired bus
- originally to interact within small num. of devs (radio/TV tuning, …)
- speeds:
  - 100 kbps (standard mode)
  - 400 kbps (fast mode)
  - 3.4 Mbps (high-speed mode)
- data transfers: serial, 8-bit oriented, bi-directional
- master/slave relationships with multi-master option (arbitration)
- master can operate as transmitter or receiver
- addressing: 7bit or 10bit unique addresses
- device count limit: max. capacitance 400 pF

Standard Mode

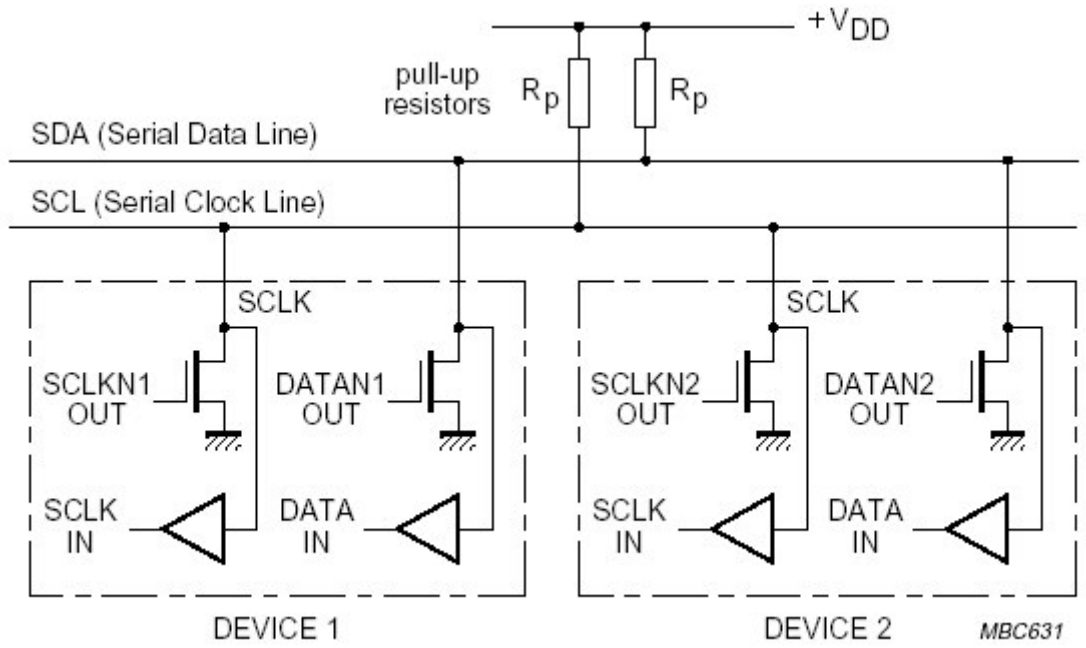
Wires and Signals

- two-wired bus
  - serial data line (SDA)
  - serial clock line (SCL)
- voltage levels
  - HIGH 1
  - LOW 0
  - not fixed, depends on associated level of voltage
- bit transfer (level triggered)
  - SCL = 1 $\Rightarrow$ SDA = valid data
  - one clock pulse per data bit
  - stable data during high clocks
  - data change during low clocks



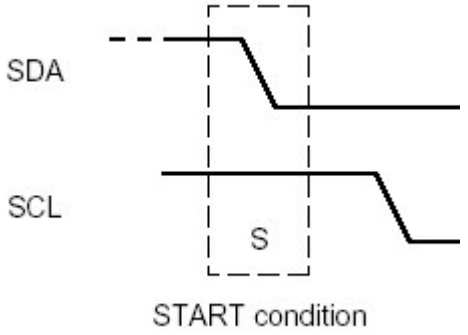
Wired-AND connection

- bus is free ⇒ SDA and SCL are high
  - by pull-up resistors
- device output is ANDed with signal on bus



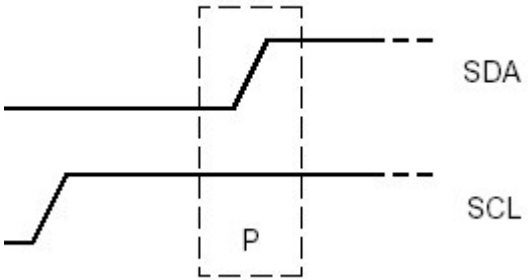
Frame

- start condition (S)
  - SDA 1→0 transition when SCL = 1
- stop condition (P)
  - SDA 0→1 transition when SCL = 1



START condition

- repeated start (Sr)
  - start is generated instead of stop
- bus state
  - busy … after S and before next P
  - free … after P and before next S



STOP condition

Masters and Slaves

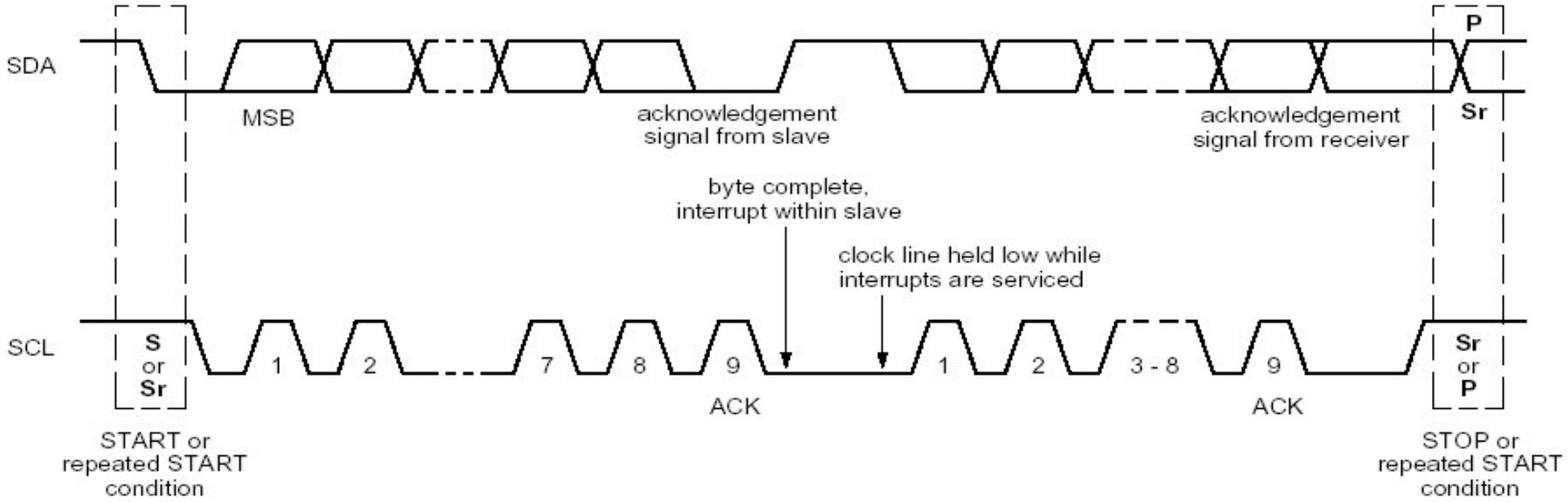
- Master device
  - controls the SCL
  - starts and stops data transfer
  - controls addressing of other devices
- Slave device
  - device addressed by master
- Transmitter/Receiver
  - master or slave
  - master-transmitter sends data to slave-recevier
  - master-receiver requires data from slave-transmitter

Data Transfer

- data bits are transferred after start condition
- transmission is byte oriented
- byte = 8 bits + one acknowledge bit
- most significant bit (MSB) first
- slave address is also datum
  - first byte transferred
  - during the first byte transfer:
    - master is transmitter
    - addressed slave is receiver
  - next bytes: depends on the last bit in address byte

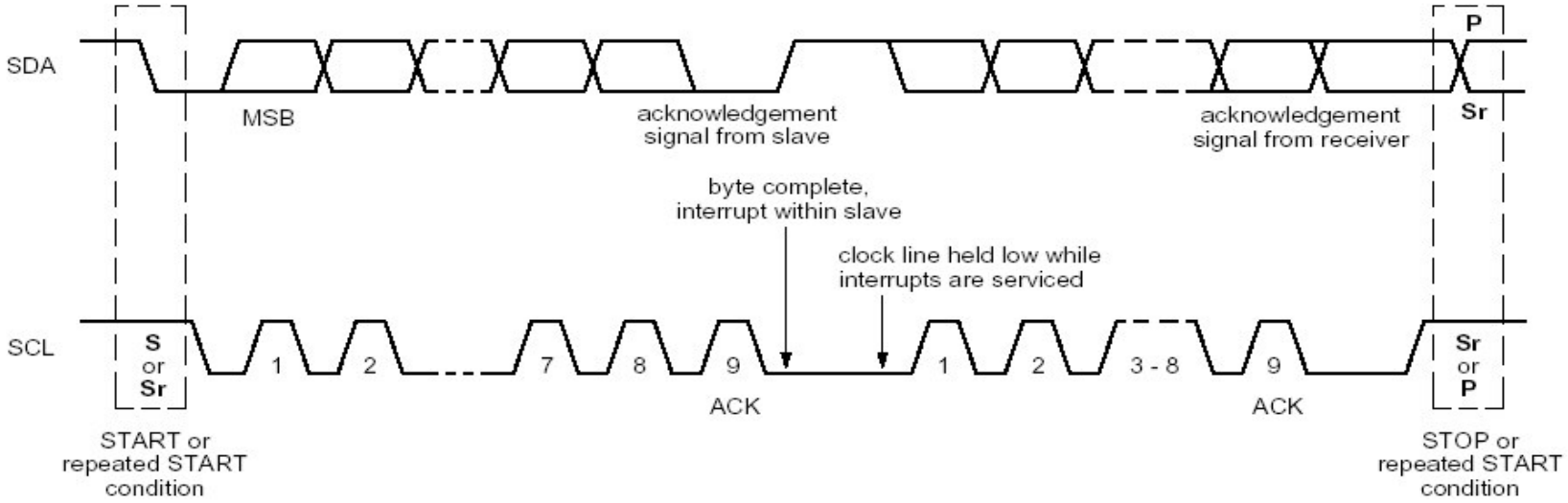
Data Transfer - SCL

- master sets SCL = 0 and generates pulse for each data bit
- 8 pulses for data bits are followed by one pulse for ack. bit
- after ack.
  - master tries to generate next byte's first pulse
  - slave can hold SCL low → master switches to wait state



Data Transfer - SDA

- data bits are generated by transmitter as SCL pulses
- 9-th pulse:
  - transmitter releases SDA
  - receiver must hold SDA low in order to ack. received data
  - slave must release SDA after ack. bit (allows master to end frame)

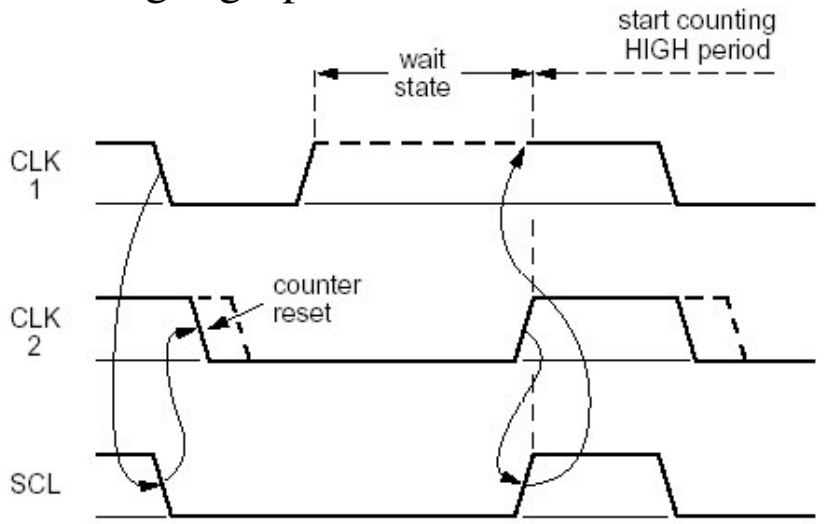


Multiple Masters

- more bus controllers can be connected
- several masters can start frame at once
- synchronization needed on SCL
- arbitration needed on SDA
- using wired-AND connection to SCL/SDA

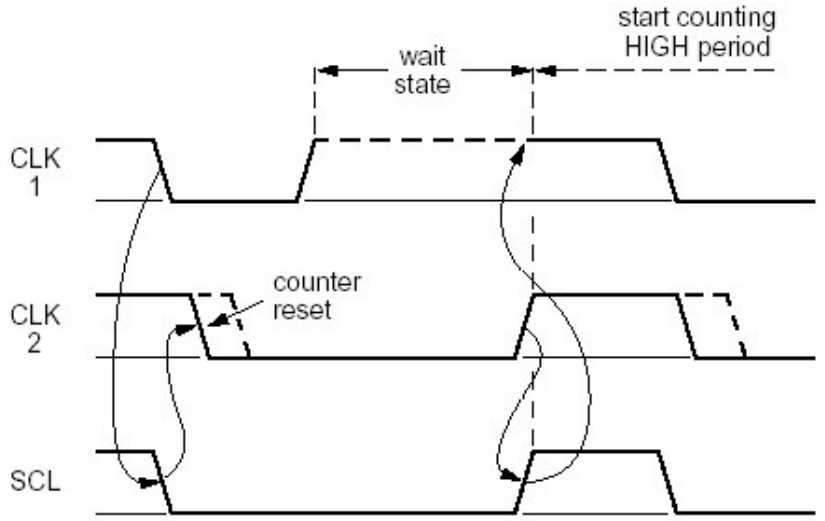
Synchronization on SCL

- frame started → SCL = 1
- first 1→0 transition (*)
  - involved masters restart their clocks
  - master holds 0 until its low-period is over
- master finished its low-period
  - releases SCL
  - SCL = 0 → switches to wait state, waits for SCL = 1
  - SCL = 1 or waiting finished → starts counting high-period
- first master finished its high-period
  - sets SCL = 0
  - equivalent to (*) state



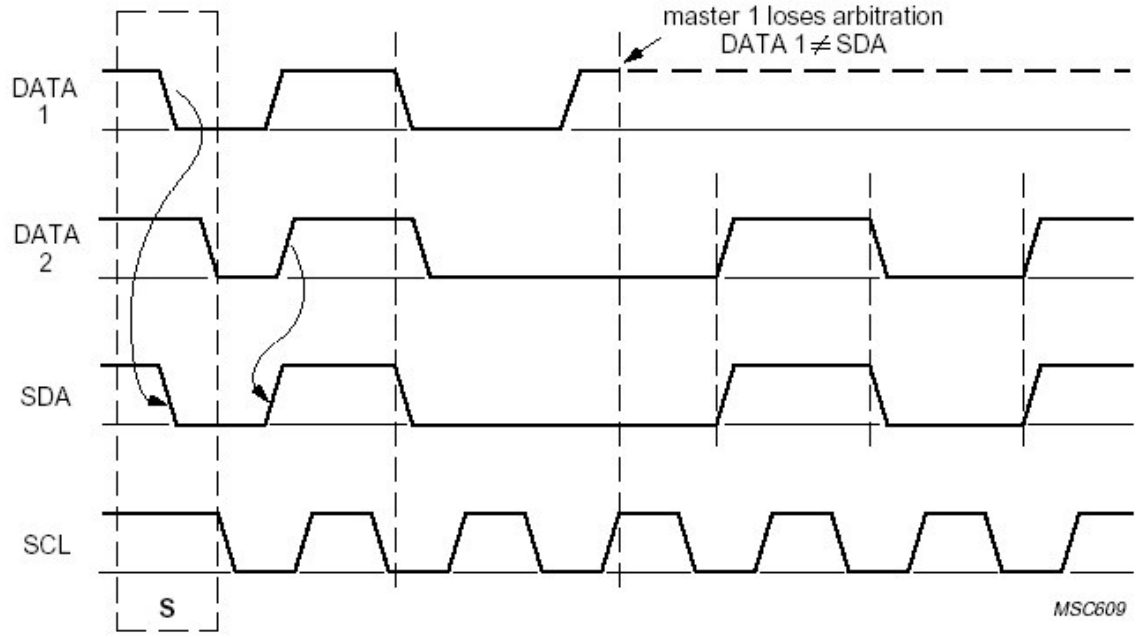
Synchronized Clocks

- low-period
  - determined by max{low-periods of involved masters}
- high-period
  - determined by min{high-periods of involved masters}



Arbitration on SDA

- frame started, SCL synchronized → high periods = valid data
- each master generates its data
- master aborts if there is another level on SDA than it generates
  → it loses arbitration, releases SDA and tries again when bus is free



Notes on Arbitration

- can continue for many bits
- adresses are compared at first stage
- if the same slave is addressed in the same mode (R/W):
  - masters are transmitters → data-bits are compared
  - masters are receivers → acknowledge-bits are compared
- if arbitration is not over before stop or repeated start:
  - comparation not allowed: stop-data, repeated start-data, stop-repeated start
  - involved masters must generate stops/repeated starts in the same positions

- loser can generate SCL pulses for synchronization until the byte is over
- losing master which can be also a slave
  - must switch immediately to slave mode

Addressing by 7 bits

- the first byte transmitted by master:
  - 7 bits: address
  - 1 bit: direction (R/W)

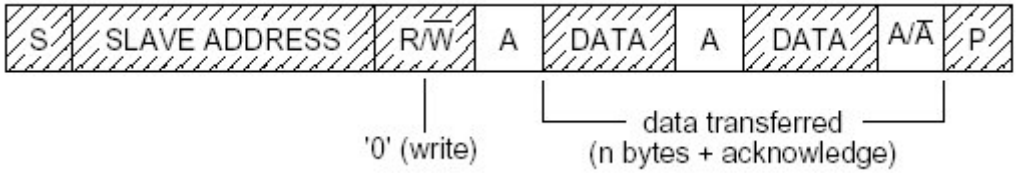
    0 … master writes data (W), becomes transmitter

    1 … master reads data (R), becomes receiver
- data transfer terminated by stop condition
- master may generate repeated start and address another device
- each device listens to address
  - address matches its own → device switches state according to R/W bit

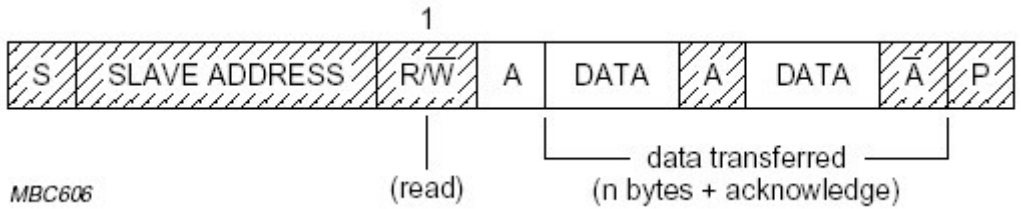
- address = fixed part + programmable part
  - fixed part assigned by I^2C committee

Frame Formats

master-transmitter



master-receiver (since second byte)



from master to slave

from slave to master

A = acknowledge (SDA LOW)

Ā = not acknowledge (SDA HIGH)

S = START condition

P = STOP condition

Special Addresses

- general call — 0000 000 | 0
- start byte — 0000 000 | 1
- CBUS address — 0000 001 | *
  - used for cooperation of I^2C and CBUS
- High-speed mode master code — 0000 1** | *
- 10-bit slave addressing — 1111 0** | *

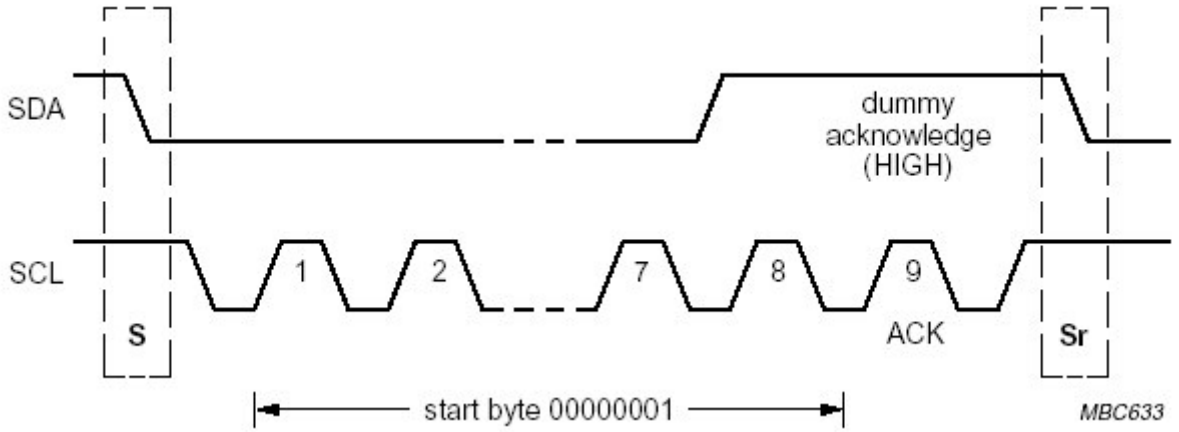
General Call

- addresses all devices
- device ignores call → not acknowledges address
- device accepts call → acknowledges address
- R/W = 0 (W) → master-transmitter, slave-receiver

- command in the second byte
- LSB = 0 (least significant bit)
  - programmable part of device's address manipulation
  - resetting devices
- LSB = 1
  - master (e.g. keyboard scanner) doesn't know where to send data
  - remaining 7 bits contain master's address

Start Byte

- device connection to bus:
  - fast
    - on-chip hardware I^2C bus interface
    - device interrupted by requests from bus
  - slow
    - no hardware interface
    - software bus monitoring (polling)
- longer start procedure needed
    - start condition, first byte = 0000 0001, ack., repeated start condition
    - fast device ignores, slow device can use lower sampling rate to detect frame start

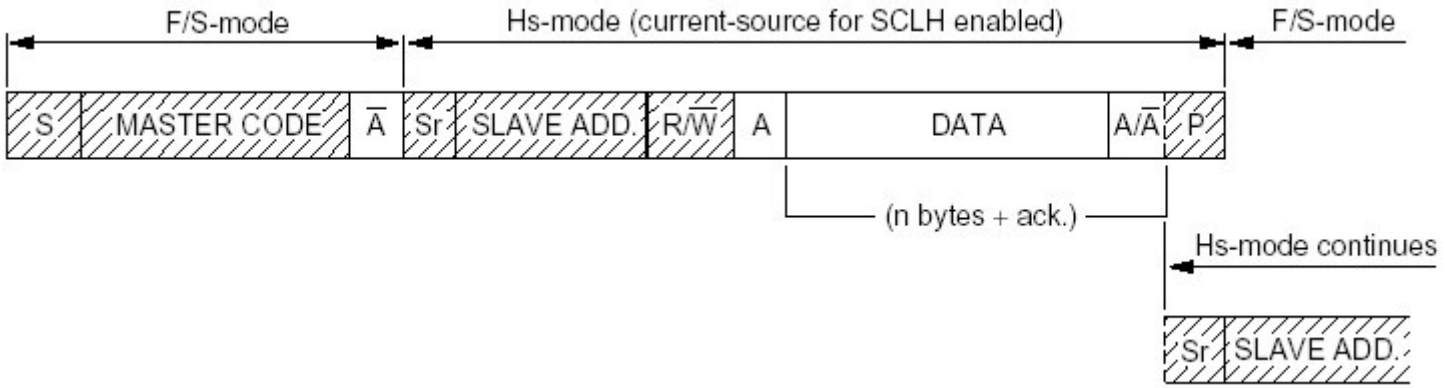


Extensions

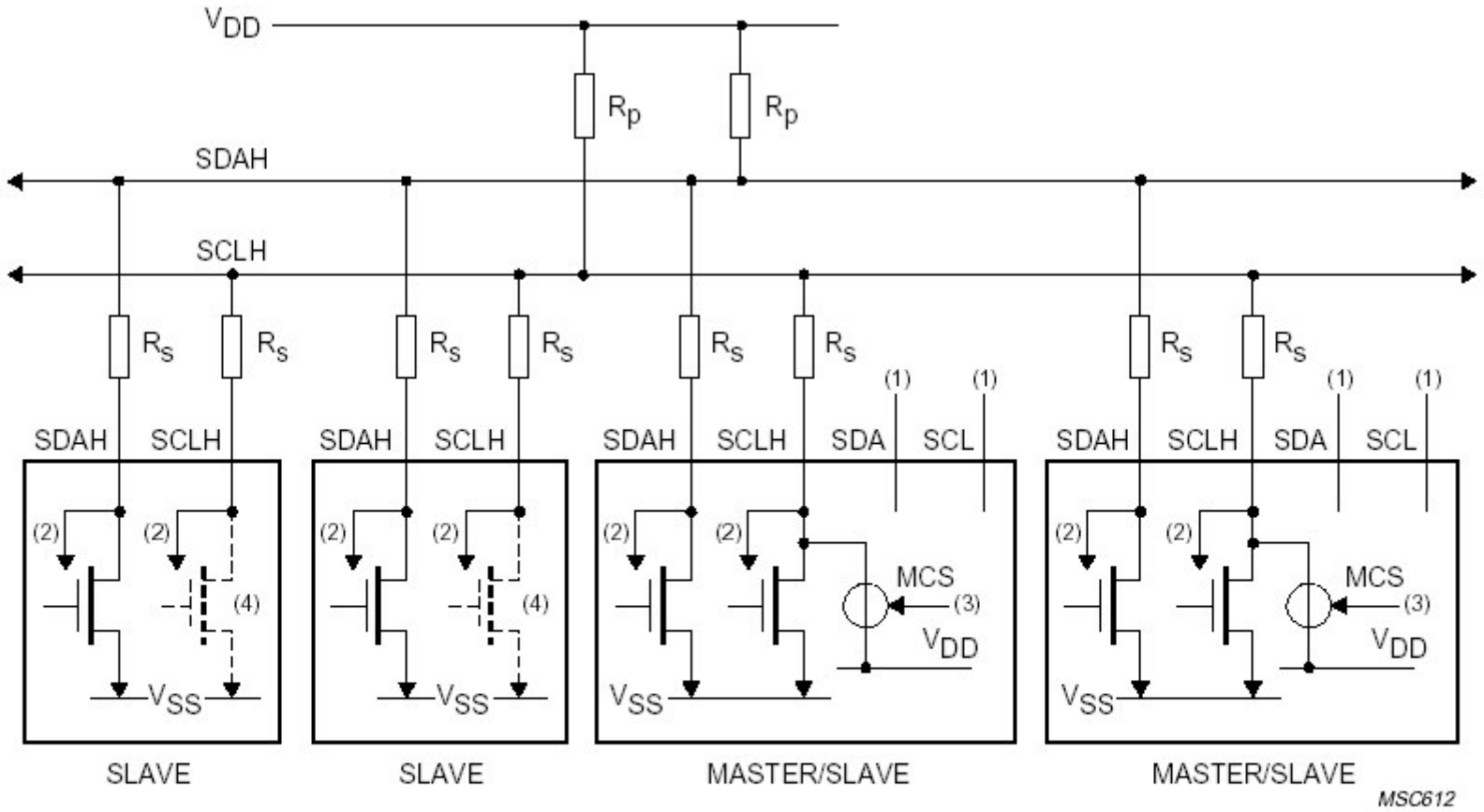
- standard mode
  - speed limit: 100 kbps, address space limit: 112 addresses
- improvements
  - fast mode (up to 400 kbps)
  - high-speed mode (up to 3.4 Mbps)
  - 10-bit addressing – can be mixed with 7-bit one (special address)
- Fast mode
  - unchanged: frame format, logic levels, max. capacitance
  - faster devices must be able to synchronize at 400 kbps
  - downward-compatible, can communicate with standard mode devices
  - not compatible with CBUS
  - changed timing

High-speed mode

- downward compatible with Standard mode and Fast mode
- same frame format
- neither synchronization nor arbitration performed during data transfer
  - arbitration always finishes before data bits transfer
  - master code arbitrates (special 7-bit address: 0000 1***)
    - unique → max. 8 masters
    - software programmable
  - master code signals HS mode data transfer
- HS devices connection to bus differs
- wires: SDAH, SCLH



HS-device Connection



(1) SDA and SCL are not used here but may be used for other functions.

(2) To input filter.

(3) Only the active master can enable its current-source pull-up circuit

(4) Dotted transistors are optional open-drain outputs which can stretch the serial clock signal SCLH.

Further Information

The I2C Bus Specification, version 2.1, January 2000
http://www.semiconductors.philips.com/buses/i2c